Euroform Polo Español

Escuela Politécnica Superior
Universidad Autónoma de Madrid
Ctra. Colmenar Km.15,
28039 Madrid, España

Seminar Invitation

Advanced FPGA Design & Verification Seminar

Innovation and Productivity: Recapturing the FPGA Advantage

Date: Friday, April 17th 2009
Location: Universidad Autonoma de Madrid, Spain
Time: 9.00am - 1.30pm

Are your FPGA projects taking too long? Now that FPGA devices have grown into hugely capable Programmable SoC's in their own right, have design methods struggled to keep up? You are invited by Synopsys to a half day seminar on Advanced FPGA Design and Verification to help find ways to recover the full benefits of FPGA-Design.

You will learn how to adopt more powerful, more productive and more predictable FPGA design and verification techniques, whether you use FPGA in your final product or only for ASIC prototyping. The seminar will introduce Synopsys tools for advanced FPGA users, including Model-based DSP algorithmic design, IP integration tools, tightly coupled constraint and analysis environments, integrated synthesis and placement and on-board Assertion-based Verification linked to RTL simulation.

Summary Agenda (9.00 to 1.30pm)

- Welcome and Introduction Synopsys and the Synplicity Business Group
- High-level Design for DSP and other Algorithms Demonstration of Synplicity DSP
- FPGA Implementation Solutions Performance, Integration and productivity
- Introduction to verifying designs in FPGA
- Demonstration of Identity
- Q&A
- Lunch - Networking with speakers and attendees

For more information, venue address and to register please click at https://events.synopsys.com
Spaces are limited so please register early in order to avoid disappointment.