VIV-ESS: Design with Xilinx FPGAs: Vivado Design Suite Essential (3 days)

VIV-ESS: Diseño con FPGAs de Xilinx: Vivado Design Suite Essential (3 días)

Introduction: This course demonstrates timing closure techniques, such as baselining, pipelining, synchronization circuits, and optimum HDL coding techniques that help with design timing closure. This course also shows you how to debug your design using advanced capabilities of the Vivado logic analyzer. These modules also tackles the most sophisticated aspects of the Vivado Design Suite and Xilinx hardware. The knowledge enables you to use the advanced capabilities of the Vivado Design Suite to achieve design closure.

Language: The classes are in Spanish, but working material is in English (available also in English for In-Company training).

Who Should Attend?: Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs. Existing Xilinx ISE users who have no previous experience with Vivado and 7-series / UltraScale / US+ devices. Project managers of FPGA based design.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Working HDL knowledge (VHDL or Verilog), Digital design experience.

Topic Covered: These course cover the following topics and concepts.

FPGA Architecture and Methodology

- Introduction to FPGA Architecture, 3D IC, SoC – Overview of FPGA architecture, SSI technology, and SoC device architecture.
- UltraFast Design Methodology: Board and Device Planning – Introduces the methodology guidelines, UltraFast Design Methodology checklist. Design Creation guidelines.
- Clocking Resources – Describes various clock resources, clocking layout, and routing.
- I/O Logic Resources – Overview of I/O resources and the IOB property for timing closure.
- Introduction to FPGA Configuration – Describes how FPGAs can be configured.
- Configuration Process – Understand the FPGA configuration process, such as device power up, CRC check, etc.

HDL, Design Techniques and TCL

- HDL Coding Techniques – Covers basic digital coding guidelines used in an FPGA design.
- Advanced construction in VHDL. Generic, generate, configurations, functions and procedure.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Introduction to Tcl Syntax and Structure. Intro to Design Analysis Using Tcl Commands
- Using Tcl Commands in the Vivado Design Suite Project Flow.

Vivado Tool

- Introduction to Vivado Design Flows –The project flow and non-project batch flow.
- Vivado Design Suite Project Mode basics – Create project, add files, explore the Vivado IDE, and simulate the design.
- Synthesis and Implementation – Create timing constraints according to the design scenario and synthesize and implement the design. Generate and download the bitstream to the demo board.

- Basic Design Analysis in the Vivado IDE – Use the various design analysis features in the Vivado Design Suite.
- Vivado Design Rule Checks – Run a DRC report on the elaborated design to detect design issues early in the flow.
- Vivado Design Suite I/O Pin Planning layout to perform pin assignments in a design.
- Vivado IP Flow – Customize IP, instantiate IP, and verify the hierarchy of your design IP.
- Creating and Packaging Custom IP – Create your own IP and package and include it in the Vivado IP catalog.
- Using an IP Container – Use a core container file as a single file representation for an IP.
- Designing with the IP Integrator – Use the Vivado IP integrator to create a subsystem.

Timing Issues, Synchronous Design and Design Constrains

- Timing model and Static Timing Analysis (STA) in Xilinx FPGAs
- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.
- Generated Clocks – Use the report clock networks report to determine if there are any generated clocks in a design.
- I/O Constraints and Virtual Clocks – Apply I/O constraints and perform timing analysis.
- Timing Constraints Wizard
- Synchronous Design Techniques in an FPGA design.
- Vivado Timing Reports – Generate and use Vivado timing reports to analyze failed timing paths.
- Setup and Hold Timing Analysis – Understand setup and hold timing analysis.
- Timing Constraints Editor – Introduces the specific editor tool to create timing constraints.
- Report Clock Networks – In oirder to view the primary and generated clocks in a design.
- Timing Summary Report – Use the post-implementation timing summary report to sign-off criteria for timing closure.
- Clock Group Constraints – Apply clock group constraints for asynchronous clock domains.

- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.

Debugging: Simulation and Logic Analyzer, Power Estimation

- Behavioral Simulation - Performs behavioral simulation for your design.
- Use of external simulator. Examples with Mentor Model/QuestaSim
- Introduction to the Vivado Logic Analyzer – Overview of the Vivado
- Logic analyzer (former Chipscope) for debugging a design: Introduction to Triggering, Debug Cores – Understand how the debug hub core is used to connect debug cores in a design.
- HDL Instantiation Debug Probing Flow – Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- Xilinx Power Estimator Spreadsheet – Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.
- Power Analysis and Optimization Using the Vivado Design Suite – Use report power commands to estimate power consumption.

Material: Each student will have a computer with the development tools (Vivado and Vivado-HLS 2019.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

VHDL01: Diseñando con VHDL. Síntesis Lógica y Simulación para FPGAs de Xilinx

VIV-ADV: Diseño FPGA de Xilinx usando Vivado Design Suite Advance

FPGA-MAN: FPGA para directores de proyectos e Integradores de Sistemas.

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

Visit www.electratraining.org

Prices and Discounts:

VIV-ADV: 1220 € (3 days)
VIV-ESS: 1210 € (3 days)

VHDL01: 780 € (3 days)
VHDL01 + VIV-ESS: 1680 € (-16%). 5 días.
VIV-ESS + VIV-ADV: 1950 € (-20%). 6 días.
VHDL01 + VIV-ESS + VIV-ADV: 2380 € (-26%).

For more than one engineer from same company / institution additional discounts

More information and schedule at (*detalles y calendario en*) http://www.electratraining.org