VHDL01: Designing with VHDL. Logical Synthesis and Simulation for Xilinx FPGA design

VHDL01: Diseñando con VHDL. Síntesis Lógica y Simulación para FPGAs de Xilinx

Introduction: This course is a detailed introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course also introduces notions of Verilog and how to interface with VHDL.

Language: The working material is in English, but classes are in Spanish.

Who Should Attend? Digital Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: Digital design experience.

Skills Gained: After completing this training, you will know how to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines, RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Notions of Verilog, and instantiation VHDL-Verilog and vice versa.
- Create and manage designs within the Vivado Design Suite environment

Material: Each student will have a computer with the development tools (Vivado 2020.x), documentation, repository whit exercises.

Related Courses:

VIV-ESS: Diseño FPGA de Xilinx usando Vivado Suite Essential

VIV-ADV: Diseño FPGA de Xilinx usando Vivado Design Suite Advance

FPGA-MAN: FPGA para directores de proyectos e Integradores de Sistemas.

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

Visit www.electratraining.org

Prices and Discounts:

VHDL01: 780 € (2 days)
VIV-ESS: 1210 € (3 days)
VIV-ADV: 1220 € (3 days)
VHDL01 + VIV-ESS: 1680 € (-16%). 5 días.
VIV-ESS + VIV-ADV: 1950 € (-20%). 6 días.
VHDL01 + VIV-ESS + VIV-ADV: 2380 € (-26%).

For more than one engineer from same company / institution additional discounts