# *HLS01: High Level Synthesis for Xilinx FPGAs with Vivado-HLx*

## *HLS01: Síntesis de alto nivel para FPGAs de Xilinx con Vivado-HLx*

***Language:*** The classes are in Spanish, but working material is in English (available also in English at In-Company).

***Who Should Attend?*** Hardware, firmware, and system design engineers who are interested in use high-level synthesis and accelerate the hardware development process.

***Duration:*** 16 h (2 days, 8 h/day).

***Prerequisites:*** Notions of Digital and Xilinx FPGA design. C, C++ or system-C.

***Introduction:*** Digital design is moving from RTL design levels using HDLs to more productive tool that uses higher level of abstractions. The course introduces the Vivado High-Level Synthesis (HLS) tool. This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. Utilize the Vivado HLS tool to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

***Skills Gained:*** After completing this training, you will know how to:

- Enhance productivity in HW development by using the Vivado HLS tool
- Know the high-level synthesis flow and how to optimize it.
- Use the Vivado tool HLS for a first project
- Identify the importance of the testbench and use in real case
- Use directives to improve performance and area and select RTL interfaces
- Identify common coding pitfalls as well as methods for improving code for RTL/HW.
- Describe how to use OpenCV functions in the Vivado HLS tool
- Perform system-level integration of IP generated by the Vivado HLS tool

***Material:*** Each student will have a computer with the development tools (Vivado and Vivado-HLS 2019.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

***Course Outline:*** This course was updated for the new tool version including RTL as blackbox and system integration with Zynq US+.

- Introduction to High-Level Synthesis. Overview of the High-level Synthesis (HLS), Vivado HLS tool flow, and the verification advantage.
- Vivado HLS Tool Flow. Explore the basics of high-level synthesis and the Vivado HLS tool.
- Design Exploration with Directives. Explore different optimization techniques that can improve the design performance. {Lecture}
- Vivado HLS Tool Command Line Interface. Describes the Vivado HLS tool flow in command prompt mode.
- Introduction to HLS UltraFast Design Methodology. Introduces the methodology guidelines covered in this course and the HLS UltraFast Design Methodology steps.
- Introduction to I/O Interfaces xplains interfaces such as block-level and port-level protocols abstracted by the Vivado HLS tool from the C design.
- Block-Level I/O Protocols. Explains the different types of block-level protocols abstracted by the Vivado HLS tool.
- Port-Level I/O Protocols. Describes the port-level interface protocols abstracted by

the Vivado HLS tool from the C design. {Lecture, Demo, Lab}

- Port-Level I/O Protocols: AXI4 Interfaces. Explains the different AXI interfaces (such as AXI4-Master, AXI4-Lite (Slave), and AXI4-Stream) supported by the Vivado HLS tool.
- Port-Level I/O Protocols: Memory Interfaces. Describes the memory interface port-level protocols (such as block RAM, FIFO) abstracted by the Vivado HLS tool from the C design. {Lecture, Lab}
- Port-Level I/O Protocols: Bus Protocol. Explains the bus protocol supported by the Vivado HLS tool. {Lecture}
- Pipeline for Performance: PIPELINE. Describes the PIPELINE directive for improving the throughput of a design.
- Pipeline for Performance: DATAFLOW. Describes the DATAFLOW directive for improving the throughput of a design by pipelining the functions to execute as soon as possible.
- Optimizing Structures for Performance. Learn the performance limitations caused by arrays in your design. You will also learn some optimization techniques to handle arrays for improving performance.
- Data Pack and Data Dependencies. Learn how to use DATA_PACK and DEPENDENCE directives to overcome the limitations caused by structures and loops in the design.
- Vivado HLS Tool Default Behavior: Latency. Describes the default behavior of the Vivado HLS tool on latency and throughput.
- Reducing Latency. Describes how to optimize the C design to improve latency.
- Improving Area and Resource Utilization. Describes different methods for improving resource utilization and explains how some of the directives have impact on the area utilization.
- HLx Design Flow – System Integration. Describes the traditional RTL flow versus the Vivado HLx design flow.
- Vivado HLS Tool C Libraries: Arbitrary Precision. Describes the Vivado HLS tool support for the C/C++ languages, as well as arbitrary precision data types.
- Hardware Modeling. Explains hardware modeling with streaming data types and shift register implementation using the ap_shift_reg class.
- Accelerating OpenCV Applications Using Vivado HLS Video Libraries. Explains the OpenCV design flow and the Vivado HLS tool support.
- Using Pointers in the Vivado HLS Tool. Explains the use of pointers in the design and workarounds for some of the limitations.

### *Related Courses:*

Today new tools and methodologies of Xilinx FPGA design relates with High Level Synthesis (HLS). It is in the hart of Vivado-HLx and Vitis.

### *Other Xilinx Technologies courses:*

Please visit our web site.

### *Dates, location and registration:*

Visit www.electratraining.org

### *Prices and Discounts:*

HLS01: 880 €
HLS01 coming from VIV-x or SoCx: 775€ (-12%)
HLS01 coming from other Xilinx course: 792 € (-10%)

For more than one engineer from same company / institution additional discounts.