SoC-RF: Designing with the Zynq UltraScale+ RFSoC

SoC-RF: Diseñando con Zynq UltraScale+ RFSoC

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend Hardware, software, firmware, and system design engineers who are interested in fully using the Zynq UltraScale+ RFSoC devices.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Embedded Systems Development Course (SoC-ESS) or experience with embedded systems design and the Vivado Design Suite, C or C++ programming. Additionally, is highly recommended the Zynq US+ course (SoC-ZUS) and deep RF knowledge for a complete exploitation.

Introduction: This course provides an overview of the hard block capabilities for the Zynq® UltraScale+™ RFSoC family with a special emphasis on the RF Data Converter and Soft-Decision FEC blocks. The focus is on:

- Describing the RFSoC family in general
- Identifying applications for the RF Data Converter and SD-FEC blocks
- Configuring, simulating, and implementing the blocks
- Verifying the RF Data Converter on real hardware
- Reviewing power estimation to help identify the power demands of the RFSoC device in various operating modes
- Identifying proper layout and PCB considerations since the Zynq UltraScale+ RFSoC is both a high-speed and an analog and digital device.

Skills Gained: After completing this comprehensive training, you will have the necessary skills to:

- Describe in general the new Zynq UltraScale+ RFSoC family
- Identify typical applications for the RF data converters
- Describe the architecture and functionality of the RF-ADC
- Utilize the RF-ADC via configuration, simulation, and implementation
- Describe the architecture and functionality of the RF-DAC
- Utilize the RF-DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the Soft-Decision FEC hard IP
- Utilize the Soft-Decision FEC via configuration, simulation, and implementation.

Course Outline: This course covers the following topics and concepts:

- Zynq UltraScale+ RFSoC Overview

  Overview of the Zynq UltraScale+ RFSoC architecture, including brief introductions to RF, RF data converter solutions, SD-FEC solutions, driver support, and tool support.
- RF-ADC Hardware

  Covers the basics of RF-ADCs. Reviews RF-ADC architecture, functionality, interfaces, configuration, and driver support.
- RF-DAC Hardware

Covers the basics of RF-DACs. Reviews RF-DAC architecture, functionality, interfaces, configuration, and driver support.

- RFSoC Hardware

  Provides an overview of the ZCU111 board and describes board setup.

- Data Converter Design

  Describes common features, the design flow, utilizing the example design by simulation and implementation, and verifying RF data converter functionality on real hardware. Includes practice of using a software driver to modify RF data converter parameters.

- Data Converter Practice

  Provides practical RF data converter experience using the ZCU111 board evaluation tool and RF analyzer tool. Demonstrates a PYNQ-based application to validate QPSK streams. Describes RF data converter frequency planning.

- PCB Design for RFSoC Devices

  Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered.

- Soft-Decision FEC Hardware

  Covers the basics of forward error correction. Reviews SD-FEC architecture, functionality, interfaces, configuration, and AXI advanced concepts. AXI Streaming background and configuration. MicroBlaze Streaming Ports. AXI Streaming capabilities. Connecting different types of AXI IP.

Related Courses:

SoC-ZUS: Zynq UltraScale MPSoC: HW and SW aspects

SoC-ESS: Essential HW and SW of Embedded Systems Design

SoC-ADV: Advanced HW and SW of Embedded Systems Design

HLS01: High Level Synthesis for Xilinx FPGAs using Vivado-HLS

VIV-ESS: Designing FPGAs Using the Vivado design Suite Essential

VIV-ADV: Designing FPGAs Using the Vivado design Suite Advanced

Dates, location and registration:

Visit www.electratraining.org

Price & Course Packs and Discounts:

- *SoC-RF: 1380€*
- *SoC-ZUS: 1280€*
- *SoC-RF + SoC-ZUS (-20%): 2120€*
- *SoC-RF coming from SoC-ADV or SoC-ESS (-16%): 1160€*
- *SoC-RF coming from any Electratraining Course (-10%): 1240€*

For more than one engineer from same company / institution additional discounts.