SoC-ZUS: Zynq UltraScale+ MPSoC HW and SW design

SoC-ZUS: Zynq UltraScale+ MPSoC diseño HW y SW

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend Hardware, software, firmware, and system design engineers who are interested in fully using the Zynq UltraScale+ MPSoC processing platform.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Embedded Systems Development Course (SoC-ESS) or experience with embedded systems design and the Vivado Design Suite, C or C++ programming. Working knowledge of the Zynq SoC (Cortex-A9), or MicroBlaze. Conceptual understanding of embedded processing systems, including device drivers, interrupt routines, Xilinx Standalone library services, user applications. SoC-ADV course is not necessary but recommended.

Introduction: This course provides a detailed overview of the capabilities and support for the Zynq® UltraScale+™ MPSoC family from a general perspective. The emphasis is on:

- Key elements of the application processing unit (APU) and real-time processing unit (RPU)
- Power domains and their control structure. Platform management unit (PMU) capabilities
- Processing system (PS) and programmable logic (PL) connectivity
- QEMU to emulate hardware behavior
- OS implementation options, including hypervisors and various Linux implementations
- Booting and configuring a system
- System security and safty

Skills Gained: The SoC-ZUS course builds on the skills gained in the Essential Embedded Systems Design with Xilinx FPGA (SoC-ESS).

After completing this comprehensive training, you will have the necessary skills to:

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU) to make best use of their capabilities
- List the various power domains and how they are controlled
- Describe the connectivity between the processing system (PS) and programmable logic (PL)
- Utilize QEMU to emulate hardware behavior
- Distinguish between asymmetric multi-processing (AMP) and symmetric multi-processing (SMP) environments
- Identify situations when the ARM® TrustZone technology and/or a hypervisor should be used
- Effectively use power management strategies and leverage the capabilities of the platform management unit (PMU)
- Define the boot sequences appropriate to the needs of the system
- Identify mechanisms to secure and safely run the system

Course Outline: This course covers the following topics and concepts:

- Application Processing Unit. Introduction to the members of the APU, specifically the Cortex™-A53 processor and how the cluster is configured and managed.
- HW-SW Virtualization. Covers the hardware and software elements of virtualization. The lab demonstrates how hypervisors can be used.
- Real-Time Processing Unit. Focuses on the real-time processing module (RPU) in the PS,

which is comprised of a pair of Cortex processors and supporting elements.

- QEMU. Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available.
- Booting. How to implement the embedded system, including the boot process and boot image creation.
- First Stage Boot Loader (FSBL). Demonstrates the process of developing, customizing, and debugging this mandatory piece of code.
- Video. Introduction to video, video codecs, and the Video Codec Unit available.
- System Protection. Covers all the hardware elements that support the separation of software domains.
- Clocks and Resets. Overview of clocking and reset, focusing more on capabilities than specific implementations.
- AXI Interconections. Understanding how the PS and PL connect enables designers to create more efficient systems.
- ARM TrustZone Technology. Illustrates the use of the ARM® TrustZone technology.
- Multiprocessor Software Architecture. Focuses on how multiple processors can communicate with each other using both software and hardware techniques.
- Hypervisors. Description of generic hypervisors and discussion of some of the details of implementing a hypervisor using Xen.
- OpenAMP. Discusses how the OpenAMP framework can be used to construct systems containing both Linux and Standalone applications within the APU.
- Linux. Describes how to configure Linux to manage multiple processors.
- Yocto. Compares and contrasts the kernel building methods between a "pure" Yocto build and the PetaLinux build (which uses Yocto "under-the-hood").
- Open Source Library (Linux). Introduction to open-source Linux and the effort and risk-reducing PetaLinux tools.
- FreeRTOS. Overview of FreeRTOS with examples of how it can be used.
- Software Stack. Introduction to what a software stack is and a number of stacks used with the Zynq UltraScale+ MPSoC.
- PMU (Power Management Unit). Introduction to the concepts of power requirements in MPSoC and the power-saving features of the device.
- Security and Software. Defines what safety and security is in the context of embedded systems and introduces several standards.
- System Coherency. Learn how information is synchronized within the API and through the ACE/AXI ports.
- DDR and QoS. Understand how DDR can be configured to provide the best performance for your system.

Related Courses:

SoC-ESS: Essential HW and SW of Embedded Systems Design

SoC-ADV: Advanced HW and SW of Embedded Systems Design

SoC-RF: Designing with the Zynq UltaScale+ RFSoC

HLS01: High Level Synthesis for Xilinx FPGAs using Vivado-HLx

Dates, location and registration:

Visit www.electratraining.org

Price & Course Packs and Discounts:

- *SoC-ZUS: 1280€*
- *SoC-RF: 1380€*
- *SoC-RF + SoC-ZUS (-20%): 2120€*
- *SoC-ZUS coming from SoC-ADV or SoC-ESS (-16%): 1075€*
- *SoC-ZUS coming from any Electratraining Course (-10%): 1152€*

For more than one engineer from same company / institution additional discounts.