SoC-ADV: Advanced HW and SW for Embedded Systems Design

SoC-ADV: Sistemas Embebidos en FPGA de Xilinx: HW y SW Avanzado

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend Hardware, software, firmware, and system design engineers who are interested in fully using the Zynq extensible processing platform.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Embedded Systems Development Course (SoC-ESS) or experience with embedded systems design and the Vivado Design Suite, C or C++ programming. Working knowledge of the UltraScale+ MPSoC processors (Cortex-A53), Zynq SoC (Cortex-A9), or MicroBlaze. Conceptual understanding of embedded processing systems, including device drivers, interrupt routines, Xilinx Standalone library services, user applications, and boot loader operation.

Introduction: Learn how to use advanced components of embedded systems design for architecting a complex system in the Zynq UltraScale+ MPSoC, Zynq System on a Chip (SoC), or MicroBlaze soft processor. Hands-on labs provide experience with:

- Developing, debugging, and simulating an embedded system
- Utilizing memory resources and Implementing high-performance DMA
- Improving designs by using the Vivado IP Integrator and download designs to board.
- Implementing an effective Zynq SoC boot design methodology
- Creating an FSBL image for flash
- Utilizing advanced Cortex-A9/A53 processor services
- Analyzing the DMA controller in the Zynq and Zynq UltraScale+
- Examining the various library services for peripherals such as Ethernet and USB controllers
- Develop a Simple Linux image using PetaLinux tools

The Advanced HW and SW of Embedded Systems Design (SoC-ADV) course builds on the skills gained in the Essential Embedded Systems Design with Xilinx FPGA (SoC-ESS).

Skills Gained: After completing this comprehensive training, you will have the necessary skills to:

- Assemble an advanced embedded system taking advantage of the various features of the Zynq UltraScale+ MPSoC, Zynq SoC, and MicroBlaze, including the AXI interconnect, and the various memory controllers
- Apply advanced debugging techniques, including the use of the Vivado logic analyzer tool for debugging an embedded system and HDL system simulation of processor-based designs
- Identify the steps involved in integrating a memory controller into an embedded system using the Cortex and MicroBlaze processors
- Integrate an interrupt controller and interrupt handler into an embedded design
- Design a flash memory-based system and boot load from off-chip flash memory
- Implement an effective Zynq SoC boot design methodology
- Create an appropriate FSBL image for flash
- Identify advanced Cortex-A9/A53 processor services for fully utilizing the capabilities of the Zynq devices.

- Analyze the operation and capabilities of the DMA controller in the Zynq MPSoC
- Describe the Standalone library services available for low-speed peripherals, Ethernet and USB controllers that are contained in the Zynq MPSoC / SoC PS
- Create a PetaLinux project to configure and build a Linux Image. Understand what is an embedded Linux kernel, a device tree and the device driver architecture. Access to PL core using user space I/O (UIO) framework

Topics Covered: This course covers the following topics and concepts:

- Reminder of Embedded Hardware Development, Software Flow with SDK, including how the compiler and linker behave, basics of makefiles, DMA usage, and variable scope.
- More details in Zynq UltraScale+, MPSoC Zynq-7000, Processor architecture.
- Debugging: Hardware Introduction for in-chip testing of hardware designs. Marking Nets (to monitor nets without having to explicitly instantiate ILA cores). Hardware-Software Co-Debugging (Cross-Triggering), describes how to enable events in hardware to pause the software and breakpoints in software to cause an ILA trigger.
- Memory Types and operation: Overview of the different types of memory available. Block RAM Controllers. Static Memory Controllers. Introduction to DDRx Memory Operation. Dynamic Memory Controller (Zynq-7000 Device) key behaviors.
- Interrupts. In deep concept of interrupts, terminology, and implementation. Interrupts in Zynq devices from both a hardware and software perspective. General Interrupt Controller (GIC), its features, and some examples of its use.
- AXI advanced concepts. AXI Streaming background and configuration. AXI Streaming capabilities. Connecting different types of AXI IP.
- DMA operation of various IP that supports DMA and DMA-like functionality. DMA block design and the DMA interrupts. Concepts behind reading and writing DMA.
- PS-PL Interface in Zynq and Zynq MPSoC Device discussing the various connection points between the PS and PL.
- PS Peripherals: Introduction to High-Speed (USB and Gigabit Ethernet) and Low-Speed (CAN, I2C, SD/SDIO, SPI and UART).
- QEMU: Introduction to the Quick Emulator, which allow to run software for the Zynq device when hardware is not available.
- Booting. Overview of booting Zynq devices and MicroBlaze processors. Boot Memory Technologies. Low-level view of the booting process. PS Processors, the concepts behind a single-core boot, a multi-core boot, and symmetric or asymmetric processing. Configuring the PL at boot. Secure Boot. Introduction to the FSBL (First Stage Boot Loader). Flash Image Generator tool.
- Sharing PS Resources (Hardware Perspective). How a master in the PL can leverage resources within the PS.
- Processor Caching, SCLR (System-Level Control Register) and NEON Co-Processing.
- Accelerator Coherency Port (ACP). Purpose and general behavior
- Linux. Embedded Linux Overview and the PetaLinux Tools. Device Drivers, User Space I/O, and Loadable Kernel Modules. Accessing Hardware Devices from User Space
- Multi-Processor Hardware Architecture. Support for cross-processor communications. Introduction to OpenAMP

Related Courses:

SoC-ESS: Essential HW and SW of Embedded Systems Design

HLS01: High Level Synthesis for Xilinx FPGAs using Vivado-HLS

SoC-RF: Designing with the Zynq UltraScale+ RFSoC

VIV-ESS: Designing FPGAs Using the Vivado design Suite Essential

VIV-ADV: Designing FPGAs Using the Vivado design Suite Advanced

Dates, location and registration:

Visit www.electratraining.org

Price & Course Packs and Discounts:

- *SoC-ADV: 1240€*
- *SoC-ESS: 1230€*
- *SoC-ESS + SoC-ADV: (-20%): 1980€*

For more than one engineer from same company / institution additional discounts.