Taller práctico: Xilinx Versal ACAP y AI Engines

XILINX VERSAL™

Un mayor nivel de rendimiento, integración y optimización

EVENTO LIVE ONLINE Y PRESENCIAL

ElectraTraining, en colaboración con Xilinx, presenta el mayor evento de formación en Xilinx Versal ACAP:

- Conoce los componentes básicos de la nueva plataforma de Xilinx, Versal ACAP, que permiten implementar aceleradores para un amplio abanido de aplicaciones
- Descubre las funciones exclusivas de Versal, los AI Engines y la Network-on-Chip (NoC), y aprende a usar Vitis Unified Software
- Explora las posibilidades que proporciona la plataforma y las herramientas de Versal para optimizar el rendimiento de tu aplicación
- Evento para desarrolladores de software y hardware, arquitectos de sistemas y cualquier persona que desee aprender cómo construir aplicaciones inteligentes y adaptables con Versal ACAP
- Formato “blended learning” (aprendizaje combinado). Dos días live-online y un día presencial en nuestras instalaciones en la Universidad Autónoma de Madrid.

FORMULARIO DE REGISTRO

Parte1: lunes 27 y martes 28 de septiembre de 2021 14:00 a 18:00h (live-online)
Introduction. Talks about the need for Versal devices and gives an overview of the different Versal families.
Architecture Overview. Provides a high-level overview of the Versal architecture, illustrating the various engines available in Versal ACAP.
Design Tool Flow. Maps the various engines in the Versal architecture to the tools required and describes how to target them for final image.
Adaptable Engines (PL). Describes the logic resources available
Processing System. Reviews the Cortex™-A72 processor APU and Cortex-R5 processor RPU that form the Scalar Engine. The platform management controller (PMC), processing system manager (PSM), I/O peripherals, and PS-PL interfaces are also covered.
PMC and Boot and Configuration. Describes the platform management controller, platform loader and manager (PLM), boot and configuration.
SelectIO Resources. Describes the I/O bank, SelectIO™ interface, and I/O delay features.
Clocking Architecture. The clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skew.
AI Engine, DSP58 and NoC Introduction. A first Introduction

Parte2: jueves 30 de septiembre de 2021 10:00 a 18:00h (presencial)
Software Build Flow. Provides an overview of the different build flows, such as the do-it-yourself, Yocto Project, and PetaLinux tool flows.
Software Stack. Reviews the Versal ACAP bare-metal, FreeRTOS, and Linux software stack and their components.
Timers, Counters, and RTC. Provides an overview of timers and counters, including the system counter, triple timer counter (TTC), watchdog timer, and real-time clock (RTC).
DSP Engine. Describes the DSP58 slice and compares the DSP58 slice with the DSP48 slice. DSP58 modes are also covered in detail.
AI Engine. Discusses the AI Engine array architecture, terminology, and AIE interfaces. Reviewing the data movement between AI Engines, between AI Engines via memory and DMA, and between AI Engines to PL
NoC Introduction and Concepts. Covers the reasons to use the network on chip, its basic elements, and common terminology.
Device Memory. Describes the available memory resources, such as block RAM, UltraRAM, LUTRAM, embedded memory, OCM, and DDR. The integrated memory controllers are also covered.
Programming Interfaces. Reviews the various programming interfaces in the Versal ACAP.
Application Partitioning. Covers what application partitioning is and how the mapping of resources based on the models of computation can be performed.

Parte 1 “Intro Xilinx Versal ACAP”: 2 días live-online – **85 €** (USD 99)
Parte 2 “More Versal, NoC+AIE”: 1 día presencial – **210 €** (USD 249)
Curso completo: Parte 1 + Parte 2 – **255 €** (USD 299)

Capacidad limitada (16 asistentes en presencial, 32 para el live-on-line)
Becas disponibles

Promoción especial de Electratraining con el patrocinio de Xilinx

Electra training

Adaptable. Intelligent.