VIT-ACC: Accelerating Applications with the Vitis Unified Software Environ

VIT-ACC: Aceleración de Aplicaciones usando el entorno de desarrollo Vitis

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Anyone who needs to accelerate their software applications using FPGAs, SoCs (such as Zynq®-7000 SoCs, Zynq UltraScale+™ MPSoCs), and Versal ACAPs.

Duration: 24h (3 days, 8 h/day).

Prerequisites: Basic knowledge of Xilinx FPGA architecture; Comfort with the C/C++ programming language. Understand typical software development flow.

Introduction: Learn how to develop, debug, and profile new or existing C/C++ and RTL applications in the Vitis™ unified software environment targeting both data center (DC) and embedded applications.

The emphasis of this course is on:

- Building a software application using the OpenCL™ API to run hardware kernels on Alveo™ accelerator cards
- Building a software application using the OpenCL API and the Linux-based Xilinx runtime (XRT) to schedule the hardware kernels and control data movement on an embedded processor platform
- Demonstrating the Vitis environment GUI flow and makefile flow for both DC and embedded applications
- Describing the Vitis platform execution model and XRT
- Describing kernel development using C/C++ and RTL
- Utilizing the Vitis analyzer tool to analyze reports
- Explaining the design methodology to optimize a design

What's New in this edition:

- Xilinx Runtime Library (XRT) Native APIs: Added new module and lab to describe the XRT native APIs—the lab also supports the Versal™ ACAP
- Xilinx Card Utilities: Added details on how the xbutil and xbmgmt utilities have been improved for this release
- Profiling: Updated the xrt.ini switches for profiling and debugging
- Optimization Methodology & C/C++ based Kernel Optimization: Updated the key techniques necessary to develop a high-performance C/C++ kernel
- Vitis Accelerated Libraries: Added information on the AI Engine DSP library, which is now part of the Vitis Libraries and is available from GitHub
- All labs have been updated to the latest software versions

Skills Gained: After completing this comprehensive training, you will have the necessary skills to:

- Describe how the FPGA architecture lends itself to parallel computing
- Explain how the Vitis unified software environment helps software developers to focus on applications
- Describe the Vitis (OpenCL API) execution model and XRT native APIs
- Analyze the OpenCL API memory model
- Create kernels from C, C++, or RTL IP using the RTL Kernel Wizard
- Apply host code optimization and kernel optimization techniques

- Move data efficiently between kernel and global memory
- Profile the design using the Vitis analyzer tool

Course outline: This course covers the following topics and concepts:

Vitis Tool Flow

- Introduction to the Vitis Unified Software Platform
- Vitis IDE Tool Overview
- Vitis Command Line Flow

Basics of Hardware Acceleration

Alveo Data Center Accelerator Cards

- Alveo Data Center Accelerator Cards Overview
- Getting Started with Alveo Data Center Accelerator Cards

Vitis Execution Model and XRT

- Vitis Execution Model and XRT
- Xilinx Runtime Library (XRT) Native APIs
- Synchronization
- Xilinx Card Utilities

NDRange

- Introduction to NDRanges
- Working with NDRanges

Design Analysis

- Profiling
- Debugging

Kernel Development

- Introduction to C/C++ based Kernels
- Using the RTL Kernel Wizard to Reuse Existing IP as Accelerators

Optimization Methodology Guide

- Optimization Methodology
- C/C++ based Kernel Optimization
- Host Code Optimization
- Optimizing the Performance of the Design

Libraries

- Vitis Accelerated Libraries

Platform Creation

- Creating a Vitis Embedded Acceleration Platform (Edge)

Alveo Data Center Accelerator Cards

- Alveo Accelerator Card Ecosystem
- Xilinx Real-Time Video Server Appliance

Related Courses:

VIT-ACC: Accelerating Applications with the Vitis Unified Software Environ

VIT-AI: Developing AI Inference Solutions with the Vitis AI Platform ment

HLS01: High Level Synthesis for Xilinx FPGAs using Vivado-HLS

SoC-ESS: Essential HW and SW of Embedded Systems Design

SoC-ADV: Advanced HW and SW of Embedded Systems Design

VIV-ESS: Designing FPGAs Using the Vivado design Suite Essential

VIV-ADV: Designing FPGAs Using the Vivado design Suite Advanced

Dates, location and registration:

Visit www.electratraining.org

Price & Course Packs and Discounts:

- *VIT-AI: 795 €*
- *VIT-ACC: 1155€*
- *VIT-AI + VIT-ACC: (-20%): 1560€*

For more than one engineer from same company / institution additional discounts.