VIV-ADV: Design with Xilinx FPGAs: Vivado Design Suite Advanced

VIV-ADV: Diseño con FPGAs de Xilinx: Vivado Design Suite Advanced (3 días)

Introduction: This course demonstrates timing closure techniques, such as baselining, pipelining, synchronization circuits, and optimum HDL coding techniques that help with design timing closure. This course also shows you how to debug your design using advanced capabilities of the Vivado logic analyzer. These modules also tackle the most sophisticated aspects of the Vivado Design Suite and Xilinx hardware. The knowledge enables you to use the advanced capabilities of the Vivado Design Suite to achieve design closure.

Language: The classes are in Spanish, but working material is in English (available also in English for In-Company training).

Who Should Attend? Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Intermediate HDL knowledge (VHDL or Verilog), Solid digital design background. The knowledge from Vivado Essential (VIV-ESS)

Software Tools: Vivado ML edition 2021.x

Topic Covered: This course cover the following topics and concepts.

FPGA Architecture and Methodology

- UltraFast Design Methodology: Implementation and Design Closure methodology guidelines covered in this course.
- Pipelining – Use pipelining to improve design performance.
- Inference – Infer Xilinx dedicated hardware resources by writing appropriate HDL code.
- Configuration Modes – Understand various configuration modes and select the suitable mode for a design.
- Daisy Chains and Gangs in Configuration – Introduces advanced configuration schemes for multiple FPGAs.
- Bitstream Security – Understand the Xilinx bitstream security features such as readback disable, bitstream encryption, and authentication.
- Introduction to High Level Synthesis Tools (Vivado-HLS) and the integration in Vivado Flow.
- Overview of Embedded System Design Technics and tools in an FPGA design Flow.

Advanced HDL, Design Techniques and TCL:

- Revision Control Systems in the Vivado Design Suite – Use version control systems with Vivado design flows.
- Scripting in Vivado Design Suite Non-Project Mode – Write Tcl commands in the non-project batch flow for a design.
- Managing Remote IP – Store IP and related files remote to the current working project directory.
- Advanced TCL features. Introduction to the Xilinx Tcl Store. Procedures, list, and regexp (regular expressions) in Tcl Scripting. Debugging and Error Handling in Tcl Scripts.
- Manipulating Design Properties Using Tcl – Query your design and make pin assignments by using various Tcl commands.

Advanced Vivado ML Tool:

- Vivado Design Suite Non-Project Mode – Create a design in the Vivado Design Suite non-project mode.
- Hierarchical Design – Overview of the hierarchical design flows in the Vivado Design Suite.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks.
- Design Analysis and Floorplanning – Explore the pre- and post-implementation design analysis features of the Vivado IDE.
- Congestion - Identifies congestion and addresses congestion issues.
- Incremental Compile Flow – Utilize the incremental compile flow when making last-minute RTL changes.
- Physical Optimization – Use physical optimization techniques for timing closure.
- Vivado Design Suite ECO Flow – Use the ECO flow to make changes to a previously implemented design and apply changes to the original design.

Timing Issues, Synchronous Design and Design Constrains:

- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Synchronization Circuits – Different technics for clock domain crossings.
- Report Clock Interaction – Use the clock interaction report to identify interactions between clock domains.
- Report Datasheet – Use the datasheet report to find the optimal setup and hold margin for an I/O interface.
- I/O Timing Scenarios – Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.
- System-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.
- Source-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.
- Timing Constraints Priority – Identify the priority of timing constraints.

Debugging: Simulation and Logic Analyzer, Power Estimation

- Timing Simulation – Simulate the design post-implementation to verify that a design works properly on hardware.
- Netlist Insertion Debug Probing Flow - Covers the netlist insertion flow of the debug using the Vivado logic analyzer.
- Sampling and Capturing Data in Multiple Clock Domains - Overview of debugging a design with multiple clock domains that require multiple ILAs.
- JTAG to AXI Master Core – Use this debug core to write/read data to/from a peripheral connected to an AXI interface in a system that is running in hardware.
- Debug Flow in an IP Integrator Block Design – Insert the debug cores into IP integrator block designs.
- Remote Debugging Using the Vivado Logic Analyzer – Use the Vivado logic analyzer to configure an FPGA, set up triggering, and view the sampled data from a remote location.
- Vivado Design Suite Debug Methodology – Understand and follow the debug core recommendations.
- Trigger and Debug at Device Startup – Debug the events around the device startup.
- Trigger Using the Trigger State Machine in the Vivado Logic Analyzer and Debugging the Design Using Tcl Commands
- Dynamic Power Estimation Using Vivado Report Power – Use an SAIF (Switching Activity Interface Format) file to determine accurate power consumption for a design.
- Power Management Techniques – Identify techniques used for low power design.

Material: Each student will have a computer with the development tools (Vivado and Vivado-HLS 2019.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

VHDL01: Diseñando con VHDL. Síntesis Lógica y Simulación para FPGAs de Xilinx

VIV-ESS: Diseño FPGA de Xilinx usando Vivado Design Suite Essential.

FPGA-MAN: FPGA para directores de proyectos e Integradores de Sistemas.

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

Visit www.electratraining.org

Prices and Discounts:

VIV-ADV: 1290 € (3 days)
VIV-ESS: 1280 € (3 days)
VHDL01: 790 € (3 days)
VHDL01 + VIV-ESS: 1750 € (-16%). 5 días.
VIV-ESS + VIV-ADV: 2080 € (-20%). 6 días.
VHDL01 + VIV-ESS + VIV-ADV: 2490 € (-26%).

For more than one engineer from same company / institution additional discounts