VHDL01: Designing with VHDL. Logical Synthesis and Simulation for AMD FPGA design

VHDL01: Diseñando con VHDL. Síntesis Lógica y Simulación para FPGAs de AMD - Xilinx

Introduction: This course is a detailed introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course also introduces notions of Verilog and how to interface with VHDL.

Language: The working material is in English, but classes are in Spanish.

Who Should Attend? Digital Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs.

Duration: 20 h (2.5 days, 8 h/day).

Prerequisites: Digital design experience.

Skills Gained: After completing this training, you will know how to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines, RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the AMD-Xilinx FPGA
- Notions of Verilog, and instantiation VHDL-Verilog and vice versa.
- Create and manage designs within the Vivado Design Suite environment

Course Outline:

- Introduction to VHDL
- VHDL Design Units. VHDL Objects, Keywords, and Identifiers
- Scalar Data Types and Composite Data Types
- VHDL Operators
- Concurrency in VHDL. Concurrent Assignments. Processes and Variables
- Control Structures in VHDL: if/else, case
- Sequential Looping Statements
- Delays in VHDL: wait Statement
- Introduction to the VHDL Testbench
- VHDL Assert Statementszxcvuytre67
- VHDL Attributes
- Vivado Simulator Good Coding Practices (VHDL)
- VHDL Subprograms, VHDL Functions, and VHDL Procedures
- VHDL Libraries and Packages
- Interacting with Simulation
- Finite State Machine Overview. Mealy and Moore FSMs

- FSM Coding Guidelines
- Writing a Good Testbench
- Targeting AMD FPGAs and Adaptive SoCs

Material: Each student will have a computer with the development tools (Vivado 2023.x), documentation, repository with exercises.

Related Courses:

VIV-ESS: Diseño FPGA de Xilinx usando Vivado Suite Essential

VIV-ADV: Diseño FPGA de Xilinx usando Vivado Design Suite Advance

FPGA-MAN: FPGA para directores de proyectos e Integradores de Sistemas.

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

Visit www.electratraining.org

Prices and Discounts:

VHDL01: 980 € (2.5 days)
VIV-ADV: 1290 € (3 days)
VIV-ESS: 1280 € (3 days)
VHDL01 + VIV-ESS: 1945 € (-14%). 5.5 días.
VIV-ESS + VIV-ADV: 2125 € (-17%). 6 días.
VHDL01 + VIV-ESS + VIV-ADV: 2770 € (-22%).

For more than one engineer from same company / institution additional discounts